

**Remarks**

The present application contains claims 86-87 and 100, as well as new claims 206-225.

In the Office Action mailed March 12, 2003, claims 85-87 and 100 were rejected under 35 U.S.C. 102(b) as being anticipated by Jacobsen (U.S. No. 5,673,131).

As the examiner is aware, Jacobsen discloses circuits 144 on the cylindrical surface of fiber optic strands 130, 132. In rejecting the claims, the Examiner rejected applicants' arguments that "the substrates of Fig. 9B of Jacobsen are ... not chips" for two reasons. The first was that the claims did not claim the limitations on the meaning of the word "chip" that are found in the definition of "chip" in The New IEEE Standard Dictionary of Electrical and Electronic Terms. The IEEE Dictionary defines a chip as "A small unpackaged functional element made by subdividing a wafer of semiconductor material. Sometimes referred to as a 'die.'" The second reason given for the Examiner's rejection was that Jacobsen's statement that the integrated circuit components on the fiber optic cylinders could be transistors, diodes, semiconductors, etc. constituted a disclosure of non-planar semiconductor chips that are designed to be cylindrical in shape.

In response to this rejection, applicants have deleted claim 85 and have amended claims 86 and 100 to better

distinguish applicants' invention from Jacobsen following the suggestions made by the Examiner. In particular, claim 86 has been amended to specify that the first and second semiconductor chips are both planar, that the first subset of electronic devices is co-planar and that the second subset of electronic devices is co-planar. Claim 100 has been revised to specify a method of capacitively coupling signals between first and second planar chips, each chip having a plurality of planar half-capacitors.

In specifying in claims 86 and 100 that the chips are planar, applicants distinguish over Jacobsen, which discloses devices built on cylindrical fiber optic strands. Further, in specifying in claim 86 that the first set of electronic devices is co-planar and that the second set of electronic devices is co-planar, applicants further distinguish over Jacobsen, which discloses non-planar devices on the cylindrical surface of a fiber optic strand. Likewise, in specifying in claim 100 that the half-capacitors are planar, applicants distinguish over Jacobsen.

For these reasons claims 86 and 100 clearly define over Jacobsen, which does not disclose or suggest the use of planar structures. Dependent claim 87 is patentable for at least the same reason claim 86 is patentable.

New claims 225-244 are substantially identical to the issued claims of U.S. Patent No. 6,500,696, and are being added to the present application to ensure compliance with 35 U.S.C. 135(b). It is applicants' intent to provoke an interference with the '696 patent, upon receiving an indication of allowability from the Examiner. Given that the present application enjoys an effective filing date six years earlier than the '696 patent, applicants clearly have the superior right to these claims.

WHEREFORE, applicants respectfully request allowance of claims 86-87, 100, and 206-225.

Respectfully submitted,

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Clean Copy of All Pending Claims

1-85. (cancelled).

86. (amended) A method of coupling signals between electronic devices in a modular electronic system, said method comprising the steps of:

    locating a first co-planar subset of said electronic devices on a first planar semiconductor chip;

    locating a second co-planar subset of said electronic devices on a planar second semiconductor chip; and,

    aligning and affixing said first and second chips so as to capacitively couple said first and second chips.

87. (original) A method of coupling signals between electronic devices in a modular electronic system as defined in claim 86 wherein the first and second chips are affixed to a base substrate thereby capacitively coupling said first and second chips via substrate.

88-99. (cancelled).

100. (amended) A method of capacitively coupling signals between first and second semiconductor planar chips, each said chip having a plurality of planar half-capacitors, said method comprising the steps of:

    affixing said first planar chip to a substrate;

    aligning said second planar chip to said first chip; and,

affixing said second planar chip to said substrate, thereby capacitively coupling corresponding half-capacitors on said first and second planar chips and providing direct capacitive coupling between said first and second planar chips.

101-205. (cancelled).

206. (new) A method of fabricating an integrated circuit module, comprising:

providing a plurality of first dice, said first dice each having half-capacitors formed on a surface thereof;

providing a plurality of second dice, said second dice each having half-capacitors formed on a surface thereof; and

arranging said first dice so that each of said first dice overlaps at least three of said second dice, and each of said second dice overlaps at least three of said first dice, thereby defining overlap areas,

wherein at least some half-capacitors of said plurality of first dice are configured to be capacitively coupled to corresponding half-capacitors of said second dice in said overlap areas.

207. (new) The method of claim 206 wherein providing said plurality of first dice and second dice include forming a dielectric layer on some of said first dice and second dice, so that half-capacitors in said overlap areas are spaced apart.

208. (new) The method of claim 206 wherein said plurality of first dice are rectangles.

209. (new) The method of claim 208 wherein said plurality of second dice are rectangles.

210. (new) The method of claim 208 wherein said plurality of second dice are squares.

211. (new) The method of claim 206 wherein said plurality of first and second dice are shaped as octagons.

212. (new) The method of claim 206 further comprising:

arranging said first dice to form a first two-dimensional repeating pattern; and

arranging said second dice to form a second two-dimensional repeating pattern.

213. (new) The method of claim 206 further comprising:

capacitively coupling some half-capacitors of said first dice to some half-capacitors of said second dice in said overlap areas.

214. (new) A method of fabricating an integrated circuit module, comprising:

providing a plurality of first dice, said first dice each having first half-capacitors formed on a surface thereof;

providing a plurality of second dice, said second dice each having second half-capacitors formed on a surface thereof; and

arranging said first dice so that each first die overlaps at least two of said second dice, thereby defining overlap areas, wherein said first half-capacitors located in said overlap areas are configured to be capacitively coupled to some of said second half-capacitors,

wherein said first dice or said second dice have raised areas relative to said surfaces, the raised areas of each of said first or said second die contacting an area on one of the overlapping die.

215. (new) The method of claim 214 wherein each of said first dice and said second dice have raised areas relative to said surfaces, and the signals pads in said overlapping areas are disposed in between said raised areas.

216. (new) The method of claim 214 wherein each of said raised areas of said first dice contact one of the raised areas of said second dice.

217. (new) The method of claim 214 wherein said plurality of first dice are on a plane that is above each of said plurality of second dice.

218. (new) The method of claim 214 wherein the plurality of first dice comprises half-capacitors that do not overlap one of the plurality of second dice.

219. (new) The method of claim 214 wherein arranging said first dice further comprises arranging said first dice so that each first die overlaps at least three of said second dice.

220. (new) A method of fabricating an integrated circuit module, comprising:

providing a plurality of first dice, said first dice each having half-capacitors formed on a surface thereof;

providing a plurality of second dice, said second dice each having half-capacitors formed on a surface thereof;

arranging said first dice so that each first die overlaps at least four of said second dice, thereby defining overlap areas; and

aligning said first dice so that half-capacitors thereof located in said overlap areas are configured to be capacitively coupled to some half-capacitors of said second dice.

221. (new) The method of claim 220 wherein said plurality of first dice are on a plane that is above each of said plurality of second dice.

222. (new) The method of claim 220 wherein each of the plurality of first dice comprises four sides, and each of said first dice overlaps one of said plurality of second dice on each of said four sides of said first dice.

223. (new) The method of claim 220 wherein the plurality of first dice comprises half-capacitors that do not overlap one of the plurality of second dice.

224. (new) The method of claim 220 wherein at least some of said half-capacitors in said plurality of first dice are capacitively coupled to a chip substrate within said first dice.

225. (new) The method of claim 220 wherein at least some of said half-capacitors in said plurality of first dice are coupled to a chip substrate through vias within said first dice.